



DX-LR20-900M22SP

Development board user's manual

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Updated records

Version	Date	Instructions	Author
V1.0	2024/10/21	Initial version	SML
V2.0	2024/11/28	Optimizing parameters	SML

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1. Introduction to hardware

DX-LR20-900M22SP is a LoRa development kit, which is independently developed and built by SHEN ZHEN DX-SMART TECHNOLOGY CO.,LTD,. It can be used with DX-LR20-900M22S module, the development board uses STM32F103C8T6 master chip, and uses SPI drive DX-LR20-900M22S. The master chip of the development board has high performance, low power consumption and rich peripheral interfaces.

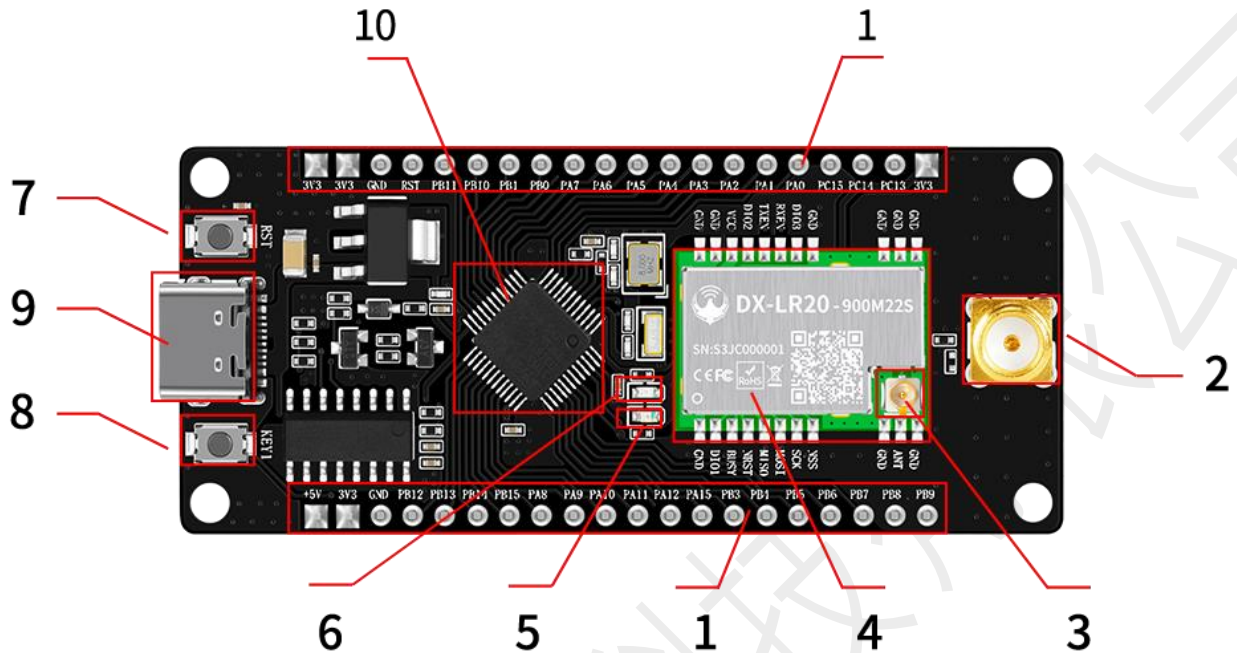


Figure 1: Development board section definition 1

Table 1: Description sheet of Development board section definition 1

Pin serial number	Pin name	Pin function
1	Baseboard pins	See Table 2 below for the bottom plate pin Definition Illustration table
2	Baseplate antenna seat	Connect antenna (2,3 can only connect one)
3	Module antenna seat	Connect antenna (2,3 can only connect one)
4	Module	DX-LR20-900M22S
5	Power indicator	Power on and always on
6	PC13	User-defined features
7	RESET	Reset
8	KEY	User-defined
9	TYPE C	Power supply, serial download
10	MCU	STM32F103C8T6

2. Suggested development environment

For easy access to sample code and free code validation, you need the appropriate tools, which are recommended as follows:

- PC system: Windows10 is recommended
- MCU integrated development environment: keil5, STM32F1xxMDm
- Burning mode: typc data cable (serial port burning)
- Debugging tools: Serial port assistant (log debugging information)

3. Sample file structure










 .vscode	2025/4/15 17:52	文件夹
 Core	2025/4/15 17:52	文件夹
 Driver	2025/4/15 17:52	文件夹
 LR_driver	2025/4/15 17:52	文件夹
 Main	2025/4/15 17:52	文件夹
 Project	2025/4/15 17:52	文件夹
 quequ	2025/4/15 17:52	文件夹
 SDK	2025/4/15 17:52	文件夹
 Readme.txt	2025/4/15 16:31	文本文档

Figure 2: Sample file2



- Core: A core file extracted from the SDK for easy modification
- Driver: A user written peripheral driver file
- LR_driver: lora (LLCC68, SX1262 public) RF driver file, currently downloaded from Semtech official website
- Main: main function file, and configuration file
- Project: The project file that contains the target binary
- queue: This file is the queue spi interface, add path and reference can be called, demo used for UART data processing
- SDK: CMSIS and HAL library, only contains the used library, add other peripherals need to add the corresponding library
- Readme.txt: Project specification file

4. Quick demo

4.1. Hardware connections and software features

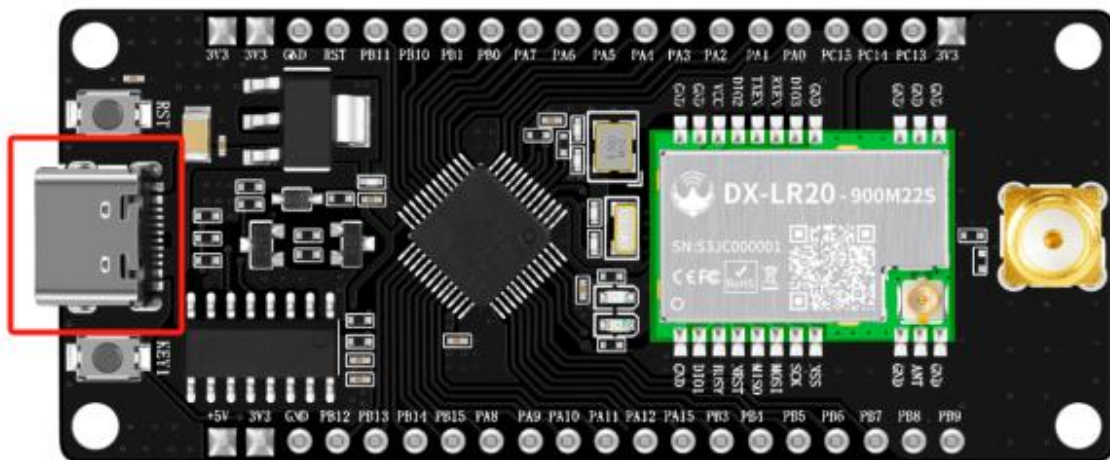


Figure 3: Hardware connectivity

- Development board has burned default open source programs (note: two development boards are needed to properly demonstrate data transfer)
- You only need to connect the typc interface to receive serial data or to burn the program of STM32F103 (UART burning).
- All the pins on the STM32F103IC have been elicited (refer to 6.2 for the specific pin definition), which is convenient for the development of other functions
- Use the serial port assistant in the data package, the default baud rate is 9600

5. Wireless module driver porting method

5.1. Typical driver library usage method

名称	修改日期	类型	大小
Core	2025/4/15 17:52	文件夹	
Driver	2025/4/15 17:52	文件夹	
LR_driver	2025/4/15 17:52	文件夹	
Main	2025/4/15 17:52	文件夹	
Project	2025/4/15 17:52	文件夹	
quequ	2025/4/15 17:52	文件夹	
SDK	2025/4/15 17:52	文件夹	
Readme.txt	2025/4/15 16:31	文本文档	2 KB

Figure 3: Typical driver libraries

The file in path: LR_driver\src is the driver of lora, which is downloaded from semtech. Only the modification of the STM32F103 adaptation HCL library is made, and other changes are not



made. The `sx126x_hal.c` file is the file that directly interacts with the LORA module for data interaction and control. In theory, when porting, it can be adapted to the new IC by modifying this part.

Path: The `UserConfig.c/` file under `LR_driver` is a public file generated when the IC driver is adapted, including some configurations of SPI, `dio1` pins, etc., which can be used when modified during transplantation.

6. Application interface

6.1. Development board pin definition

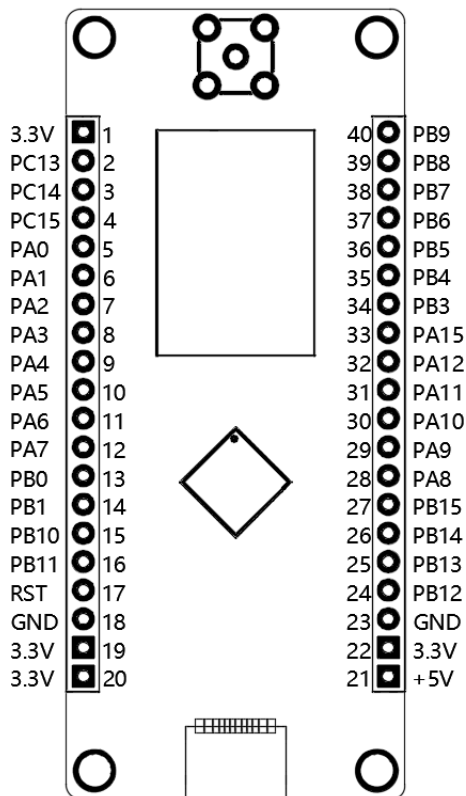


Figure 3: Development board pin definition

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6.2. Description of the development board pin definition

Table 2: Development board pin Definition Description Table 2

Pin serial number	Pin name	Pin function	Instructions
1,19,20,22	3.3 V	3.3V power supply	-



2,3,4,5,6,7,8,13,14,15,16,24,25,26,27,28,31,32,33,34,35,36,37,38,39,40	PC13,PC14,PC15,PA0,PA1,PA2,PA3,PA4,PA5,PA6,PA7,PA9,PA10,PA11,PA12,PA15,PB0,PB1,PB10,PB11,PB12,PB13,PB14,PB15,PA8,PA11,PA12,PA15,PB3,PB4,PB5,PB6,PB7,PB8,PB9	IO port	User-defined
9	PA4	NSS	Module pieces select pins for starting an SPI communication
10	PA5	SCK	SPI clock input pin
11	PA6	MISO	SPI data output pin
12	PA7	MOSI	SPI data input pin
17	RST	Reset	-
18,23	GND	Power ground	-
21	+5V	5V power supply	-
29	PA9	TX	Send data
30	PA10	RX	Receive data

6.3. Foot position connection diagram

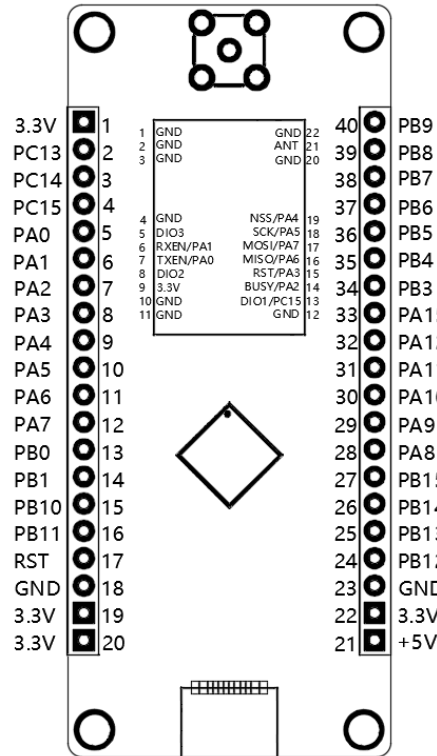


Figure 4: Foot position connection diagram4

7. Mechanical dimensions and layout suggestions

This section describes the mechanical dimensions of the development board, all dimensions are in millimeters; All dimensions not marked with tolerance, tolerance is ± 0.3 mm.



7.1. Base plate mechanical ruler

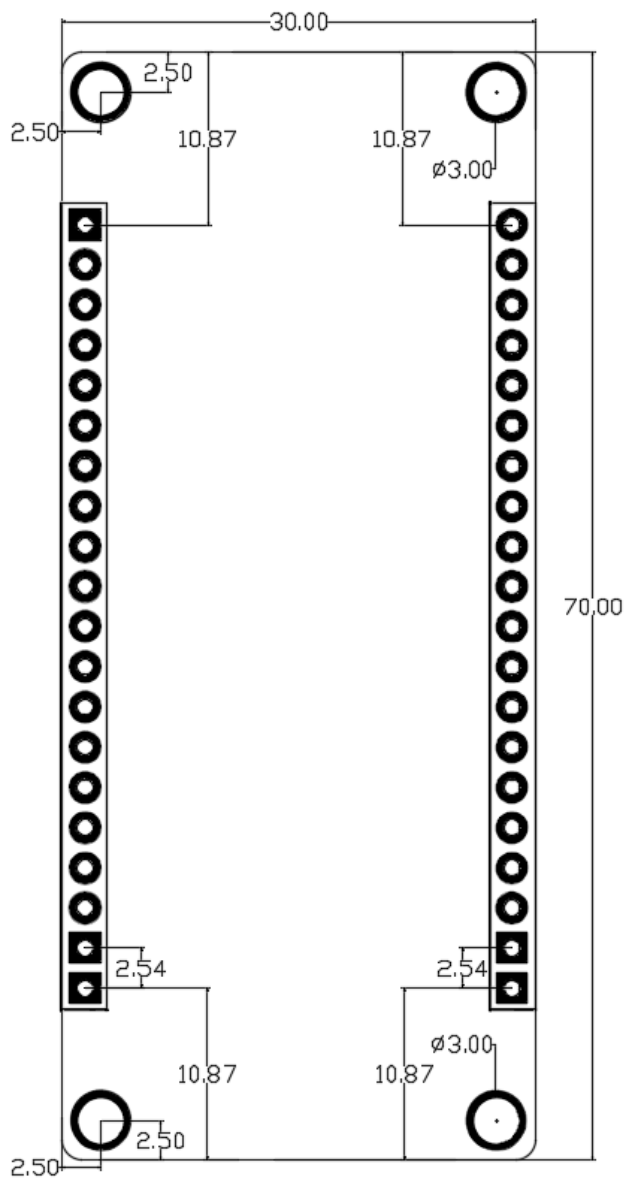


Figure 5: Bottom plate size diagram

7.2. Top/bottom view of the bottom plate

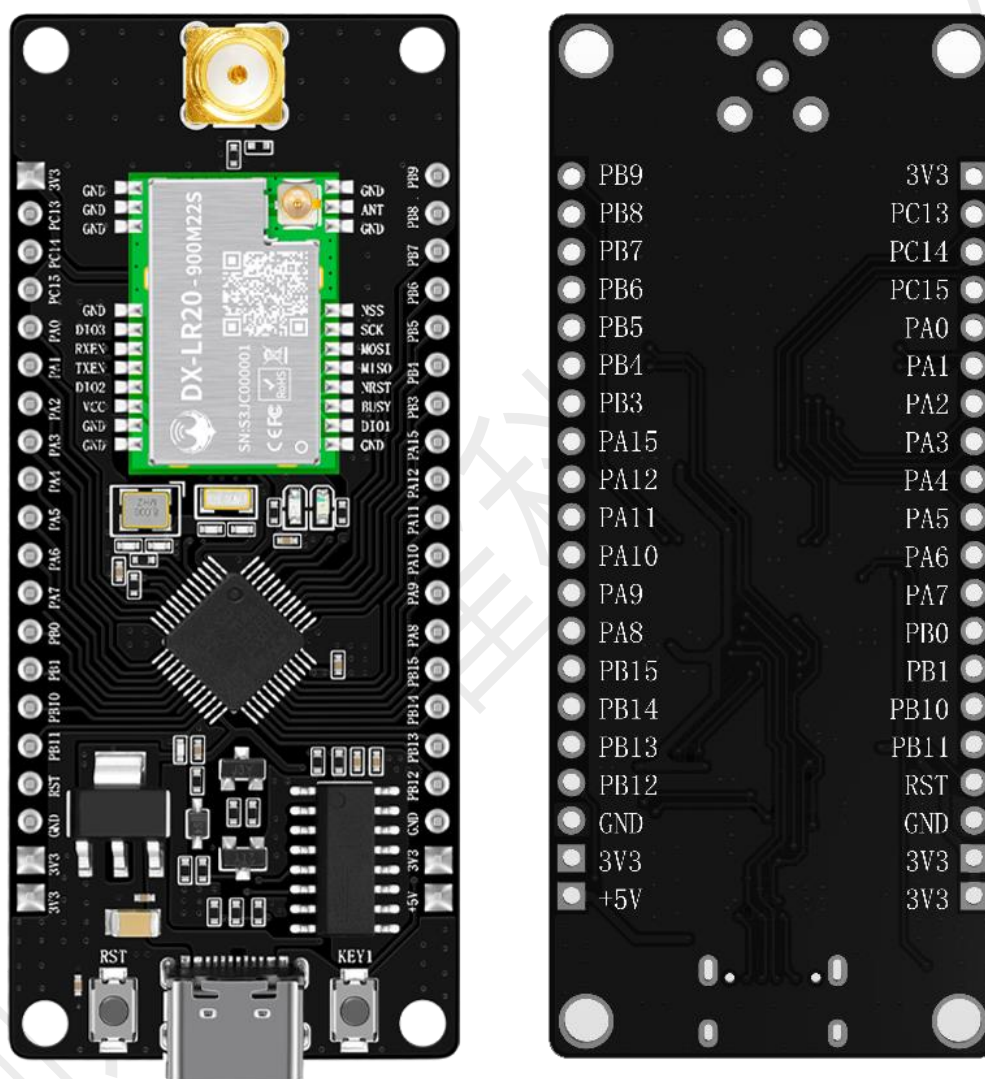


Figure 6: Bottom board top view and bottom view

Notes

The above picture is for reference only, please refer to the actual product appearance and label



information.